Modeling of CMOS Devices and Circuits on Flexible Ultrathin Chips

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Abstract—The field of flexible electronics is rapidly evolving. The ultrathin chips are being used to address the high-performance requirements of many applications. However, simulation and prediction of changes in response of device/circuit due to bending induced stress remains a challenge as of lack of suitable compact models. This makes circuit designing for bendable electronics a difficult task. This paper presents advances in this direction, through compressive and tensile stress studies on transistors and simple circuits such as inverters with different channel lengths and orientations of transistors on ultrathin chips. Different designs of devices and circuits in a standard CMOS 0.18-µm technology were fabricated in two separated chips. The two fabricated chips were thinned down to 20 µm using standard diced-before-grinding technique steps followed by post-CMOS processing to obtain sufficient bendability (20-mm bending radius, or 0.05% nominal strain). Electrical characterization was performed by packaging the thinned chip on a flexible substrate. Experimental results show change of carrier mobilities in respective transistors, and switching threshold voltage of the inverters during different bending conditions (maximum percentage change of 2% for compressive and 4% for tensile stress). To simulate these changes, a compact model, which is a combination of mathematical equations and extracted parameters from BSIM4, has been developed in Verilog-A and compiled into Cadence Virtuoso environment. The proposed model predicts the mobility variations and threshold voltage in compressive and tensile bending stress conditions and orientations, and shows an agreement with the experimental measurements (1% for compressive and 0.6% for tensile stress mismatch).

Index Terms—CAD, CMOS, device modeling, flexible electronics, thinning-down techniques, ultrathin silicon.

I. INTRODUCTION

MICROELECTRONICS has revolutionized our lives through fast communication and computing. Currently, the field is dominated by the silicon-based CMOS electronics technology. The advances in CMOS electronics have been achieved mainly through high-performance and ultralarge-scale integration enabled by miniaturization [1]. The bendability or conformability is nowadays adding a new dimension to the electronics research. A range of alternative materials such as paper, plastic, or organic semiconductor are being explored for this purpose [2]–[6] as the brittle nature of Si precludes its use in flexible electronics. These new directions are reshaping electronics industry by enabling new solutions for emerging applications such as wearable systems, electronic skin, flexible displays, and Internet of things (IoT), and so on [7]–[10].

Bendability itself is not enough as many of these emerging applications require high performances to meet the fast communication and computation requirements. For example, the communication stack in IoT will be required to handle data in frequency bands up to ultrahigh frequencies (0.3–3 GHz) [11]. Similarly, the drive electronics in fully flexible or rollable displays require high current [12]. Achieving such performances, at par with conventional CMOS ICs, appears difficult with devices from materials such as organic semiconductors. As an example, recently reported organic semiconductor-based bendable microprocessor having 4000-transistor and 8-bit logic circuit operates at a clock frequency below 10 Hz [13]. This is four orders of magnitude (100 kHz) lower than Intel 4004 introduced in 1971. This modest performance is owing to the low inherent charge carrier mobility (~1 cm²/Vs (maximum reported ~43 cm²/Vs [14]) cf. ~1000 cm²/Vs for single crystal Si) and the poor resolution of printing technologies typically used to fabricate the devices from organic semiconductors [15]. For these reasons, silicon and other high-mobility materials have caught the attention again and alternative ways of using them for flexible electronics, for example in new forms ranging from nanowires (NW) to ultrathin chips (UTCs) and so on are being explored [16]–[20].

One of the challenges for silicon-based flexible electronics (in fact for flexible electronics in general) is that the device response changes constructively of destructively as a result of bending induced stresses [21]–[23]. Mechanical stresses, either internally generated or externally applied, affect the carrier mobility, threshold voltage and so on and change the flat-band voltage (VBF) and the surface potential (Φs) [24]. For electronics design and to predict the response of circuits under different bending states it is important to understand these variations and present improved device models for future computer aided design (CAD) tools. The development of predictive,
and accurate, models for flexible devices, and their compatibility with CAD tools will be a step change in bendable ICs. A few studies reported over last few years have theoretically analyzed some of the internal (e.g., process induces stresses, as in strained silicon) [25], [26], and external (e.g., uniaxial and biaxial bending) stresses and have presented models of devices [27]–[29]. In our previous work, we also reported the compact model of nMOS, its coding in Verilog-A and compilation in Cadence environment [30]. The model predicts the mobility and threshold-voltage variations under compressive and tensile bending stress (Fig. 1). However, as in conventional electronics this may change with device size. Furthermore, at circuit level the output may be different. For example, some of the transistors in a circuit may experience increase in mobility and others may have reduced mobility (depending on the type of stresses they experience) and the overall effect could be the cancellation of bending induced variations in the response. With this background, this paper presents advances in modeling and simulation of nMOS and pMOS transistors with different channel lengths and orientations and simple circuits such as inverters.

This paper is organized as follows: a brief state-of-the-art of the recently reported bendable devices and circuits, including strained silicon-based devices is presented in Section II. The description related to the layout design, process followed for ultrathin chip, and the characterization of bendable devices and circuits is given in Section III. A detailed discussion of the analytical model of the bendable n- and p-MOSFET as well as bendable inverter, along with model validation is presented in Section IV. Finally, the key outcomes are summarized in Section V.

### II. STATE-OF-THE-ART

The fabrication and performance of the bendable silicon-based circuits along with their constitutive nMOS and pMOS response undergoing uniaxial and biaxial stress has been widely investigated in the past [21]–[23], [31]–[33]. Other techniques have also been explored with devices and circuits made from transferrable silicon nanomembranes or thin-film amorphous silicon [34], [35]. Some of the reported simple CMOS circuits on ultrathin silicon, including this paper, are summarized in Table I. Device level characterization complemented with theoretical modeling of bendable devices offers a great opportunity in the field of device modeling and simulation using CAD tools. However, despite the growing interest in the field of theoretical modeling of internally generated stresses, there are few papers on the effects of externally applied stresses, and the development of theoretical models for mechanically bendable silicon devices.

Stress engineering remains an important method to improve CMOS performance. Although, stress engineering has been extensively used in fabrication to enhance performance, the physical mechanisms behind change in carrier mobility ($\mu_e/\mu_p$) is yet to be fully understood. Starting with strained-induced changes in effective mass of carriers, a quantitative evaluation of stress-induced split of conduction band edge and experimental demonstration of changes in effective mass has been presented in [36]. There have been reports of analytical models defining the effect of stress on electronic transport of devices. The relation between normalized

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Thickness [μm]</th>
<th>Radius of Curvature [mm]</th>
<th>Bending Test Structure</th>
<th>Orientation of channel</th>
<th>Carriers’ Mobility $\mu_n/\mu_p$ [cm²/V·s]</th>
<th>Size of Transistor nMOS</th>
<th>pMOS</th>
<th>(WL) [μm]</th>
<th>Thinning Process</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ring Oscillator</td>
<td>N/A</td>
<td>N/A</td>
<td>Externally applied package strain</td>
<td>N/A</td>
<td>0.1/0.02</td>
<td>0.1/0.02</td>
<td>UTB-SOI</td>
<td>[31]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ring Oscillator Inverter</td>
<td>15</td>
<td>6.3, 15.8</td>
<td>Cylinder</td>
<td>N/A</td>
<td>132</td>
<td>80</td>
<td>0.35/0.25</td>
<td>0.45/0.25</td>
<td>0.22/0.22</td>
<td>Sequential RIE</td>
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<td>15</td>
<td>Cylinder</td>
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<td>1450</td>
<td>300</td>
<td>0.34/0.15</td>
<td>0.45/0.13</td>
<td>0.22/0.22</td>
<td>SOI wafer</td>
</tr>
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<td>30</td>
<td>0.085</td>
<td>Cylinder/Microcure cover slip</td>
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<td>158</td>
<td>396</td>
<td>134</td>
<td>0.34/0.15</td>
<td>0.45/0.13</td>
</tr>
<tr>
<td>Inverter</td>
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<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
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<td>70</td>
<td>40/500</td>
<td>40/500</td>
<td>0.35/0.35</td>
<td>0.35/0.35</td>
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<tr>
<td>Inverter</td>
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<td>20, 40</td>
<td>Cylinder</td>
<td>0° and 90° layout in [100] wafer</td>
<td>1229</td>
<td>438</td>
<td>4/0.18</td>
<td>4/0.18</td>
<td>0.35/0.35</td>
<td>DBG</td>
</tr>
</tbody>
</table>

Fig. 1. Illustration of ultrathin chips on flexible substrate under uniaxial tensile and compressive bending stress.
variation in mobility as a function of stress, device orientation, and piezoresistive coefficient has been presented by Bradley et al. [37]. In another study, Dhar et al. [38] presented an electron mobility model of the strain effects resulting in variations in both effective mass and valley degeneration. Similar studies have been reported for the theoretical modeling of holes’ mobility under variable stress [39]–[41]. Among them, Wang et al. [41] studied the energy-momentum curve to include arbitrary stress capabilities, and developed a model for quantum anisotropic transport of holes. Due to splitting of bands into subbands upon experiencing stress, the threshold voltage also experience shift from its unstressed value. Additionally, Lim et al. [42] compared the shift in the threshold voltage due to uniaxial and biaxial tensile stress.

As important as internally generated stresses are, which have been exploited to enhance the performance of silicon devices, studying the effect of externally applied bending stresses is also essential. However, there have been few works reported in this area, which have been also implemented using BSIM, PSP, and son on models. For example, Khagzar and Lueder [43] presented a static and dynamic model for amorphous silicon thin-film transistors implemented in SPICE. An exponential distribution of the deep and tail states in the energy gap has been used by taking also into account parasitic effects. A different way to perform simulations of bulk MOSFETs under uniaxial mechanical stress using BSIM3 stress-dependent parameters is presented in [27]. This paper extended and verified by ultrathin Si-chips experimental results in [28]. Mijalković [44] focused on the impact of different material properties on electrical characteristics and proposed a model, which considers the change of valence and conduction band edge energies during externally applied strain as an effective change in the semiconductor material. In another study, Alius et al. [45] included the effects of self-heating and stress in Verilog-A in order to enhance the library with the standard MOS model parameters (PSP 103.1) for IMS 0.5 μm CMOS. They modified the low- and high-field mobility, and threshold-voltage equations in order to include the contributions of bending and stress orientation versus the crystal orientation of the wafer.

Using the effective mobility and threshold-voltage parameters in the BSIM4 model, we have further extended the state-of-the-art and have developed the compact model in Verilog-A. The model is compatible with advanced standard CMOS technologies in Cadence Virtuoso. The proposed model predicts the mobility variations and threshold voltage in compressive and tensile bending stress conditions and orientations. Here, the model implemented for both the nMOS and pMOS devices using parameters extracted (e.g., oxide thickness, channel length modulation, saturation current, forward bias capacitance factor, and so on) from a standard CMOS 0.18 μm technology. Compiling the model during the schematic circuit simulation assists analog and digital designers to carry out circuit simulation under different bending stresses and orientation conditions. A detailed description of these models is presented in Section IV.

III. Layout, Fabrication, and Characterization

To demonstrate the validity of the proposed models, we designed two chips in a standard 0.18 μm CMOS technology. The chips fabricated in an external foundry were thinned down to ∼20 μm using well-established grinding technique. The thinned chips were then integrated on flexible printed circuit boards (PCB) for further study involving characterization and comparison of simulation and experimental results as given in following sections.

A. Layout

In this paper, we have designed two chips for a wider analysis of chips under bending conditions. The first design includes nMOS and pMOS transistors with fixed channel width, but two different channel lengths (0.18 and 0.35 μm). Furthermore, these devices were designed to be fabricated along two different crystal axis i.e., 0° and 90° with respect to the wafer crystal orientation, to study the variations in carriers’ mobility and threshold voltage and to include more sources of variations in our model. Channel width of nMOS and pMOS transistors are 4 and 8 μm, respectively, and the chip area is 0.9 mm × 0.8 mm. We have also designed a second chip to further advance our study of bendable compact device models toward their use in circuit simulation. This 0.9 mm × 0.788 mm size chip, shown in Fig. 2(c), includes inverter logic gates with different sizes and orientations.

B. Fabrication

The two chips discussed above were fabricated in a standard 0.18 μm CMOS technology in an external foundry using p-type wafers. The microphotograph of fabricated chips is shown in Fig. 2(a) and (b). As the thickness of chips after fabrication was about 480 μm, it is not possible to bend these chips. The bendability can be achieved by thinning down the bulk silicon from 500 μm to the ultrathin regime (<50 μm). The reduction in thickness can be achieved either by physically knocking off the material by grinding or by using chemically etching [18]. The thinning processes can be classified into chemical thinning [46], physical thinning [47], or physicochemical thinning [48]. Among these, the physical thinning gives faster material removal rate and provides smooth thin silicon after stress relieving step. In particular, back grinding using abrasive particles and embedded grinders is widely used and established technique. To ensure maximum yield percentage, dicing before grinding (DBG) [47] has been used in this paper. The silicon die was partially diced by Half-Cut dicing tool along the dicing line, as shown in Fig. 2(d). Afterward, the front side of the precut die was placed on a back-grind protective tape, while the backside was grinded slowly with coarse and fine grinding. The chips separated automatically when the grinding level reached the dicing depth. In total ten fabricated chips were thinned down to 20-μm thickness. Five of these chips include differently sized and oriented nMOS and pMOS transistors, and five chips include inverter logic gates, as discussed in Section III-B. Following this step, the thinned chip was packaged over 120-μm polyimide-based flexible
C. Characterization and Experimental Results

The mechanical characterization of ultrathin Si dies is usually carried out using a three-point or four-point-bending setup [49], [50]. In this paper, due to the small size of the die we have used high-quality 3-D printed structures for compressive (downward direction) and tensile (upward direction) bending stress, as shown in Fig. 3(a). These structures have radii of curvature 20 and 40 mm. The nominal strain at the active area of the chip when is bent at these bending radii can be calculated using the following equation:

\[ \varepsilon = \frac{d}{2R} \times 100\% \]  

(1)

where \( \varepsilon \) is the strain applied to the active area of the chip, \( d \) is the thickness of the sample, and \( R \) is the radius of bending.

Using (1), the percentage nominal strain on the surface of the chip was found to be 0.05% and 0.025% for 20 and 40 mm, respectively.

After packaging of thinned chips, the flexible PCBs were mounted on the 3-D printed structures, as is shown in Fig. 3(b)–(d). Using these structures, we evaluated the effects of bending on the transistors’ mobility and threshold voltage. The output (\( I_D-V_D \)) and transfer (\( I_D-V_G \)) characteristics of 0.18-\( \mu \)m nMOS and pMOS in both channel orientation (0° and 90°) were measured at supply voltage \( V_{DD} = 1.8 \text{ V} \).

In this paper, we have determined threshold voltage (\( V_{Th} \)) using the extrapolation in linear region method [51] from the \( I_D-V_{GS} \) characteristic at low \( V_{DS} \). The charge carrier mobility of MOSFET devices were theoretically calculated using the output characteristic (\( I_D-V_D \)) in the early saturation region.

In this region, \( I_D \) is given by [52]

\[ I_D = \frac{\mu C_{ox} W}{L} (V_{GS} - V_{Th})^2 \]  

(2)

where \( C_{ox} \) is the oxide capacitance. For nMOS devices with 0.18- and 0.35-\( \mu \)m gate length \( C_{ox} \) values are ranging from 5.18–5.72 fF/\( \mu \)m\(^2\) with typical value of 5.45 fF/\( \mu \)m\(^2\). For pMOS devices with 0.18- and 0.35-\( \mu \)m gate length \( C_{ox} \) values are ranging from 9.43 to 10.21 fF/\( \mu \)m\(^2\) with typical value of 9.82 fF/\( \mu \)m\(^2\). The threshold voltage for planar devices with channel length of 0.35 \( \mu \)m was found to be 0.41 \text{ V} for nMOS and −0.79 \text{ V} for pMOS. For devices with channel length of 0.18 \( \mu \)m, the threshold voltage was found to be 0.6 \text{ V} for nMOS and −0.5V for pMOS. The drain-current (\( I_D \)) depends both on the carrier’s mobility (\( \mu \)) and the threshold voltage (\( V_{Th} \)), and as reported by Lim et al. [42] shift in threshold voltage is observed upon experiencing strain. During characterization of devices with 0.35-\( \mu \)m channel length, we measured a change of ∼30 mV in threshold voltage as a result of bending.

The changes in charge carriers’ mobility during compression and tension are given in Table II. The observed trend in Table II is in agreement with previously reported
Fig. 4. Measured (symbols) and simulated (lines) transfer and output characteristic curves of nMOS and pMOS transistors in linear scale under planar, tensile, and compressive bending conditions. nMOS 0.18-μm transistor. (a) Output characteristic ($I_D$–$V_D$). (b) Transfer characteristics ($I_D$–$V_G$). pMOS 0.18-μm transistor. (c) Output characteristic ($I_D$–$V_D$). (d) Transfer characteristics ($I_D$–$V_G$). nMOS 0.35-μm transistor. (e) Output characteristic ($I_D$–$V_D$). (f) Transfer characteristics ($I_D$–$V_G$). pMOS 0.35-μm transistor. (g) Output characteristic ($I_D$–$V_D$). (h) Transfer characteristics ($I_D$–$V_G$).

TABLE II

<table>
<thead>
<tr>
<th></th>
<th>Planar</th>
<th>Tension 40mm (0.025%)</th>
<th>Tension 20mm (0.05%)</th>
<th>Compression 40mm (0.025%)</th>
<th>Compression 20mm (0.05%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>1229</td>
<td>1241</td>
<td>1251</td>
<td>1167</td>
<td>1159</td>
</tr>
<tr>
<td>PMOS</td>
<td>438</td>
<td>451</td>
<td>455</td>
<td>452</td>
<td>460</td>
</tr>
</tbody>
</table>

Fig. 5. Measurement results of inverter performance in (a) planar state, under (b) 40-mm (0.025%) tension and (b) 40-mm (0.025%) compression.

$$V_{IH} = V_M + \frac{V_{DD}}{2A_0}$$
$$V_{IL} = V_M - \frac{V_{DD}}{2A_0}$$

It can be seen that the range between $V_{IH}$ and $V_{IL}$ is short in both compressive and tensile bending. This confirms that the inverters have high noise margin without compromising the performance.

IV. MODELING, SIMULATION, AND MODEL VALIDATION

Compact modeling aims to develop a numerically efficient representation of the device behavior under different modes...
of operation. With flexible electronics, the compact device models should also include the effects of mechanical bending stress. Stress effects are not a new concept in compact modeling as the substrate-induced strain that has been exploited to improve device performances. Example includes Si/Si–Ge heterostructures, which create compressive biaxial tensile stress in the order of 700 MPa in the whole wafer substrate [54]. Likewise, layout-dependent stresses, like shallow trench isolation (STI) stress, can exert more than 750-MPa compressive stress in the vicinity area changing the charge carrier mobility of devices through the band structure modification, and thus alter the threshold voltage $(V_{th})$ depending on the orientation of the doping profile [55]. Existing MOS compact models typically consider such process and layout-induced stresses, but they do not consider the stress effects in flexible electronics in terms of bending radius or bending axis.

Externally applied stresses have a different impact on the effective carriers’ mobility, and the threshold voltage with respect to other internally generated stresses discussed previously. The critical stress, at which most thin chips with thickness less than 20 $\mu$m break has been identified to be approximately 300 MPa [28]. The resistivity of silicon changes when it experiences stress, and the effect is termed as piezoresistive effect [56]. The mobility of carriers is also influenced by the crystal structure of material and the orientation of device channel [57]. In planar condition, the ellipsoidal shape of the six degenerated valleys of the conduction band structure of crystalline Si along [001], [010], and [100] crystal directions has two different curvatures and thus two effective masses [58]: longitudinal, $m_l = 0.97m_0$, and transversal, $m_t = 0.19m_0$, where $m_0$ is the free electron rest mass. The total effective mass can be written as, $m^* = \left[\frac{1}{6}(2/m_l) + \frac{4}{m_t}\right]^{-1} = 0.26 \cdot m_0$. As uniaxial or biaxial stress increases, electrons repopulate into the conduction subbands influencing the effective mass, $m^*$, and the momentum relaxation time, $\tau$. Since the mobility of carrier is inversely proportional to its effective mass and popularly written as, $\mu = (|\vec{v}|/E) = (q \cdot \tau)/(m_0 \cdot m^*)$, any change in effective mass changes the mobility and thus the resistivity. Along with mobility, the threshold voltage of MOSFETs also changes because of stress and eventually the drain current changes.

<table>
<thead>
<tr>
<th>Inverter 0.18 $\mu$m</th>
<th>$V_{th}$ (V)</th>
<th>$V_{th}$ (V)</th>
<th>$V_{th}$ (V)</th>
<th>$V_{th}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Planar</td>
<td>1</td>
<td>6.09</td>
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<td>Tension 40mm (0.025%)</td>
<td>1.03</td>
<td>5.92</td>
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<td>Tension 20mm (0.05%)</td>
<td>1.04</td>
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<td>6.01</td>
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<tr>
<td>Compression 20mm (0.05%)</td>
<td>0.98</td>
<td>5.98</td>
<td>1.131</td>
<td>0.829</td>
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</table>

To understand and predict the behavior of bendable devices, it is essential to derive analytical equations describing their performance. Based on theoretical concepts described in Sections II and IV, the experimental results, and the use of mobility and threshold-voltage parameters from BSIM4, the modified drain-current, and threshold-voltage mathematical equations of MOSFETs under different bending conditions are [30], [45]

$$I_{D_{\text{stress}}} = I_{D_0}(1 \pm \pi I_{D_0} \cdot \sigma_{I_{D_0}})$$

$$V_{th_{\text{stress}}} = V_{th_0}(1 \pm \pi V_{th_0} \cdot \sigma_{V_{th_0}})$$

where $I_{D_0}$, $V_{th_0}$, $I_{D_{\text{stress}}}$, and $V_{th_{\text{stress}}}$ are the drain current and threshold voltage of the transistor under planar condition and the effective drain current and threshold voltage of the transistor under bending conditions, respectively. The piezoresistive coefficients proportional to the drain-current and threshold voltage, denoted as $\pi I_{D_0}$ and $\pi V_{th_0}$ can be written as a function of channel orientation ($\theta$) as

$$\pi I_{D_0} = 1 - 2 \times \pi I_{D_0} \cdot \sin(\theta)$$

$$\pi V_{th_0} = 1 - 2 \times \pi V_{th_0} \cdot \sin(\theta)$$

The extracted parameters and the above equations are implemented in Verilog-A to enable circuit simulation as in standard ASIC design process. Recently, we demonstrated the applicability of (3) and (4) in Verilog-A and compiled in the Cadence environment to model the behavior of n-MOSFET [30]. Further extending that study, the compact model here takes into account the drain-current and threshold voltage, with the following equations:

$$\sigma_{I_{D_0}} = E \cdot \frac{h}{2R} \cdot \Delta G_{I_{D_0}} \left(1 + \frac{\Delta G_{I_{D_0}}}{G_{I_{D_0}}}\right)$$

$$\sigma_{V_{th_0}} = E \cdot \frac{h}{2R} \cdot \Delta G_{V_{th_0}} \left(1 + \frac{\Delta G_{V_{th_0}}}{G_{V_{th_0}}}\right)$$

The extracted parameters and the above equations are implemented in Verilog-A to enable circuit simulation as in standard ASIC design process. Recently, we demonstrated the applicability of (3) and (4) in Verilog-A and compiled in the Cadence environment to model the behavior of n-MOSFET [30]. Further extending that study, the compact model here takes into account the $I–V$ characteristics of p-MOSFETs, which allows to simulate complementary digital gate circuits such as inverter. To validate our models, we compared the experimental data with the simulation results, as shown in Fig. 4(a)–(h).

To further advance this paper, both n- and p-MOSFETs with different or same channel orientation were used to model the behavior of inverters at different radii of bending curvature. Among the major logic gates, inverter is the most basic and widely studied circuit due to its low-power consumption, and relatively high speed. The externally applied bending stress causes changes of the switching behavior by shifting the midpoint voltage $(V_M)$ of inverters, as is shown in Fig. 6(a)–(d).

As discussed in Section III-C, the experimental value of midpoint voltage $(V_M)$ for planar Inverter 0.18 $\mu$m and Inverter 0.35 $\mu$m was found 1 V, while the simulated values of $V_M$ were 1.005 V and 1.01 V, respectively. The maximum experimental percentage difference of $V_M$ during compressive and tensile stress were 2% and 4%, respectively, while the
in our proposed models for nMOS and pMOS in Verilog-A. Following that, we designed and simulated an inverting circuit in Cadence Virtuoso environment with the same operating voltage as in [21] using the modeled nMOS and pMOS transistors. In this paper, the reported midpoint voltage ($V_M$) for planar, downward (tensile), and upward (compressive) bending conditions was 0.40293 V, 0.39501 V, and 0.40539–0.40698 V, respectively. Our model validates the reported behavior of the inverter by showing similar $V_M$ values, i.e., 0.4 V for planar, and similar decreases and increases in $V_M$ for tensile and compressive bending stresses.

V. CONCLUSION AND OUTLOOK

With growing interest in flexible electronics, the need for device modeling and improved CAD tools has been felt. However, the area has been scarcely researched. The work presented in this paper will fill the gap with the improved models to predict the behavior of devices on bendable substrates. To capture many sources of variations and complexity the ultrathin chips developed with different channel length ($L = 0.18 \, \mu m$, $0.35 \, \mu m$) and orientation ($\theta = 0^\circ$, $90^\circ$) have been used. With bending, the change in mobility and shift in the threshold voltage has been observed. To simulate this change, a compact and Cadence-friendly model has been developed. The model itself is a combination of mathematical equations, and extracted parameters from the BSIM4, written in Verilog-A. The maximum observed percentage difference in drain-current during bending for nMOS was found $\sim 5.9\%$, while the percentage difference of simulated results was $4.4\%$. For pMOS it was found $\sim 2.4\%$, while the simulated difference was $2.17\%$. In the case of inverter, a maximum percentage difference of $2\%$ for compressive and $4\%$ for tensile stress was observed for the experimental midpoint voltage ($V_M$). The simulated results of $V_M$ showed a close matching with percentage difference of $1\%$ and $3.4\%$, respectively. Overall, this paper advances the state-of-the-art in the bendable silicon technology, by presenting high-performance devices and circuits with reliable functioning complemented with a compact model, which can simulate their response.

Future work will involve thinning down the chips with more complex circuits and integrating with sensors in a bendable ultrathin chip and further validate the proposed compact model. This provides the possibility of integration of ultrathin chips with sensors and readout circuits on a polymeric substrate, which could find an attractive application in electronic skin and flexible electronics.

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VILOURAS et al.: MODELING OF CMOS DEVICES AND CIRCUITS ON FLEXIBLE ULTRATHIN CHIPS


et al.  [20] H. Yoo, “Dicing before grinding process for preparation of semiconduc-


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