CMOS Vertical Hall Magnetic Sensors on Flexible Substrate

Hadi Heidari, Member, IEEE, Edoardo Bonizzoni, Member, IEEE, Umberto Gatti, Member, IEEE, Franco Maloberti, Life Fellow, IEEE, and Ravinder Dahiya, Senior Member, IEEE

Abstract—This paper presents the realization of different vertical Hall sensors (VHSs) implemented using a 0.18-μm CMOS technology and mounted on flexible substrates. Various geometries of VHS have been studied to obtain the optimum sensor device dimension and shape. COMSOL multiphysics simulation results are validated with respect to the electrical behaviour of an eight-resistor Verilog-A model implemented in Cadence environment. Simulation and measurement results are in good agreement. The use of polymeric foils and current spinning technique compensate for the effects caused by mechanical stress and possible fabrication imperfections. Measurement results for a low-offset basic VHS in planar state show a sensitivity of $59 \pm 1 \text{ V(AT)}^{-1}$ in voltage mode and of $8 \pm 0.1 \text{ %T}^{-1}$ in current mode.

Index Terms—Vertical Hall sensor, flexible substrate, mechanical stress, magnetic field, CMOS magnetic sensor.

I. INTRODUCTION

Hall effect sensors have been the workhorse magnetic sensor for a large number of applications including biosensors [1], contactless current sensors [2], and electronic compasses [3]. More recently, they have been used in flexible and wearable electronics and a series of flexible and stretchable sensors have been reported [4]–[6]. These include imperceptible giant magnetoresistive (GMR) and magnetic field sensors using Hall effect and organic field effect transistors (OFETs) [7]–[10]. The application of Hall sensors in wearables is interesting and the field will further benefit if the Hall sensors are based on CMOS technology. With CMOS devices it is easier to meet the high performance requirements such as low-power and high-speed, which are needed in many wearable systems especially for wireless communication. Furthermore, it is possible to obtain conformable and wearable CMOS magnetic sensors system using ultra-thin technology which has been reported recently [11].

This work presents CMOS Vertical Hall Sensors (VHSs) mounted on flexible polymeric substrate (Fig. 1(a)) to allow the structure to conform to curved surfaces such as the finger or the wrist of a human/prosthetic hand. The performance of VHS in four different geometries has been evaluated with sensors operated in both voltage and current mode. The low-offset basic VHS has the sensitivities of $59 \pm 2 \text{ V(AT)}^{-1}$ and $8 \pm 0.1 \text{ %T}^{-1}$ in voltage and current modes, respectively, for an applied external magnetic field range of $0$–$5 \text{ mT}$. The presented VHS is sensitive to the in-plane component of the magnetic field, $B_y$, which allows the sensor to detect a magnetic field in its plane. For better sensitivity and reduced offset, the VHS presented here uses an optimized symmetric 4-folded 3-contact (4F 3C) structure with current-spinning technique. The 4-folded structure has been chosen here as, among several possible geometries [12]–[15], this structure is known to result in high resolution and low offset performance [16], [17]. Extending the preliminary work reported in [18], this paper also presents the results from an extensive physical simulation and behavioural modelling of current-mode VHSs on flexible substrate and provides guidelines for the device size, shape, and performance optimization. The effect of substrate bending on device output has also been studied to investigate the role of piezoresistive effect in the performance of electronics [19], [20].

This paper is organized as follows. The VHS design, the numerical analysis for bendability, and the performance variations under uniaxial mechanical stress are presented in Section II. Section III gives a detailed description of the testchip architecture and the implementation of multi-sensors. This is followed by the VHS modelling and simulation results in Section IV. The experimental results collected from several prototypes fabricated with a 0.18-μm CMOS technology and integrated on flexible substrate are presented in Section V. Finally, the results and future works are summarized in the concluding Section VI.

II. CMOS VERTICAL HALL SENSORS (VHS)

A. VHS Structure

VHS devices with various types and shapes have been reported and analyzed in the past for sensitivity and offset. These include four-contact (4C), five-contact (5C), six contact (6C) and 4F 3C type VHS [16], [21]. The comparison of these structures using 3D COMSOL indicates that the current-mode 4F 3C VHS structure is the best choice and
HEIDARI et al.: CMOS VERTICAL HALL MAGNETIC SENSORS ON FLEXIBLE SUBSTRATE

Fig. 1. (a) The VHS chip mounted on a PVC foil. (b) Cross-section of the 4F 3C VHS implemented in a CMOS technology. (c) Voltage-mode configuration. (d) Current-mode configuration with biasing conditions and currents flows. Blue and red lines represent the current paths in the case of zero and non-zero magnetic field, respectively. (e) Block diagram of the test-chip. (f) Sensor configurations in the four current spinning phases.

TABLE I

<table>
<thead>
<tr>
<th>Reference</th>
<th>[12]</th>
<th>[13]</th>
<th>[14]</th>
<th>[16]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Geometry</td>
<td>8C VHS</td>
<td>5C VHS</td>
<td>5C VHS</td>
<td>4F 3C VHS</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>45 V/AT</td>
<td>1.5 %T⁻¹</td>
<td>1.525 %T⁻¹</td>
<td>1.16 %T⁻¹</td>
</tr>
<tr>
<td>Offset</td>
<td>200 μT</td>
<td>≤1 mT</td>
<td>44 mT</td>
<td>60 μT</td>
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</table>

The same has been used in this work. Other architectures such as five contacts (5C) [13], [14] and eight contacts (8C) [12] have limitations such as offset and readout complexity, as summarised in Table I. The structure of the 4F 3C VHS, shown in Fig. 1(b), has four lined up n-wells, each with three n+ contacts connected via metal lines as shown in the inset. To reduce the 1/f noise and carrier surface losses, the n+ diffusions are separated by shallow p+ diffusions.

The device has four terminals, C1, C2, C3 and C4. Assuming that a current Ibias is entering through the terminal C1 and is exiting through C3, the zero current in C2 and C4 reflects a zero magnetic field situation. When a magnetic field BX₂ is present along x₂-direction i.e. parallel to the surface, as shown in Fig. 1(b), the current flow paths are altered and a differential current, IHall, appears at the two output terminals C2 and C4. IHall, BX₂ and Ibias give a measure of the sensitivity of the Hall devices as:

\[ S_I = \left| \frac{I_{Hall}}{I_{bias} \times B_{X_2}} \right| \]  

Geometric parameters such as the shape and size of n-wells, n+, and p+ diffusions, the distance between contacts and between contacts and device edges may also influence the device performance. For example, the Hall current, IHall, (and hence the sensitivity) is inversely proportional to the n-well doping concentration and therefore n-wells with small width are typically used in VHSs. To understand the effect of geometry on device performance, VHSs with four geometries are considered in this work. These four versions, namely basic, small-distance, small-width, and deep n-well, are given in Table II and explained in following Sections.

B. VHS Mode of Operation

The VHSs reported in the literature are typically operated in voltage-mode, as shown in Fig. 1(c) [12], [21]. However, they can also be operated in the current-mode, as depicted in Fig. 1(d) [22], [23]. In fact, as explained below, the Hall sensor in current-mode exhibits better sensitivity and therefore the current-mode is preferred in this work. But, for the sake of comparison with Hall sensors reported in the literature, the performance of VHSs has also been evaluated in the voltage-mode.

In voltage-mode (Fig. 1(c)), the terminal C1 is connected to the bias voltage, VBias, and C3 is grounded. The remaining two terminals, i.e. C2 and C4, give the output voltages VHn and VHp. When an external magnetic field is applied, the

TABLE II

<table>
<thead>
<tr>
<th>VHS geometries</th>
<th>basic</th>
<th>small-distance</th>
<th>small-width</th>
<th>deep n-well</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lc [μm]</td>
<td>1.71</td>
<td>1.71</td>
<td>1.71</td>
<td>1.71</td>
</tr>
<tr>
<td>Lf [μm]</td>
<td>2.65</td>
<td>2.65</td>
<td>2.65</td>
<td>2.65</td>
</tr>
<tr>
<td>Dc [μm]</td>
<td>9</td>
<td>6</td>
<td>9</td>
<td>9</td>
</tr>
<tr>
<td>Df [μm]</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>W [μm]</td>
<td>7.44</td>
<td>7.44</td>
<td>6.2</td>
<td>11.6</td>
</tr>
<tr>
<td>d [μm]</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>
Lorentz force on the carriers leads to shortening and lengthening of current paths in C4 and C2, respectively. Due to the symmetry of the structure, the voltage at the output terminal is in the middle of both C2 and C4 (V_Hn and V_Hp) [24] and, therefore, the shortening/lengthening of the current paths is represented in terms of resistance variations. The equivalent resistances between the pairs of four terminals, (R_0 − ΔR_V), (R_0 + ΔR_V) on the top section and (R_0 + ΔR_V), (R_0 − ΔR_V) in the bottom section, are shown in Fig. 1(c). R_0 is the initial resistance between the nodes in each section when the magnetic field is zero and ΔR_V is the resistance variation in the presence of a magnetic field. The resistance of interconnections is assumed negligible. With these values, the differential Hall voltage (V_Hp − V_Hn) can be expressed as:

\[ V_{HV} = V_{bias} \frac{\Delta R_V}{R_0} \]  
(2)

In current-mode (Fig. 1(d)), the output terminals C2 and C4 are connected to the common mode voltage, V_C,M. The bias current, I_{bias}, flows in and out of the terminals C1 and C3, respectively. In this case, the differential Hall current, I_{H1}, can be calculated as:

\[ I_{H1} = 2I_{bias} \frac{\Delta R_I}{R_0} \]  
(3)

where ΔR_I is the resistance variation with respect to R_0 when a magnetic field is present. From (2) and (3), it can be noted that, for an equal variation in the resistance (i.e. for ΔR_V = ΔR_I), the sensitivity in current-mode is twice the one achieved in voltage-mode and that is why the current-mode of operation is preferred in this work.

C. CMOS Hall Sensors on Flexible Substrate

In applications such as wearable systems, the sensors often need to conform to the curved surface, which calls for their integration on flexible substrates. The integration of planar chips on flexible substrates comes with new set of challenges. For example, besides bonding of chips on flexible substrates, any deformation or bending can lead to mechanical stress induced performance variations. In the case of VHSs, the mechanical stresses lead to piezo-Hall effect, which can change the magnetic sensitivity [25]. This means that the Hall effect sensor can be used to detect magnetic field as well as the mechanical bending. However, this capability to detect multiple parameters also means that it is difficult to measure the desired parameter when multiple stimuli are simultaneously present. Therefore, the piezoresistive effect must be compensated or accounted for to accurately measure the magnetic field strength when the sensor is mechanically deformed [26], [27].

Assuming the plane-stress (i.e. \( \sigma_{33} \equiv 0 \)) the sensitivity variation with mechanical stress can be expressed as [28]:

\[ S_I(\sigma, V, T) = S_I(V, T) \cdot [1 + P_{12} \cdot (|\sigma_{11}| + |\sigma_{22}|)] \]  
(4)

where \( P_{12} \) is the piezo-Hall coefficient in \((x_1, x_2)\)-plane (\( P_{12} = 40 \times 10^{-11} \) Pa\(^{-1}\)) for a \( n \)-well with \( n = 4 \times 10^{16} \) cm\(^{-3}\) [25]), and \( \sigma_{11} \) and \( \sigma_{22} \) are the in-plane stress \( \sigma \) components along [100] and [010] axes, respectively (see Fig. 2(e)). In absence of external magnetic field and mechanical stress, all the four resistors in Fig. 1(c) have the same initial value (R_0), which is calculated as

\[ R_0 = \left( q \cdot \mu_n \cdot n \cdot H \right)^{-1} \]  
(5)

and can be determined through two steps: (i) the node C3 is grounded and a driving current is applied to the terminal C1; (ii) the terminal C1 is grounded and the current is applied to terminal C3. In (5) \( q \) is the electron charge and \( \mu_n \) is the electron mobility for \( n \)-type doping. To account for the piezo-Hall and piezoresistance induced resistance variation, the value of each resistor can be expressed as:

\[ R = R_0(1 \pm \beta |B| \pm \Pi |\sigma|) \]  
(6)
where $\beta$ is the magnetic resistance coefficient, defined as the average of initial values of resistors $R_0$ in presence and absence of magnetic field (B), and $\Pi$ is the general piezoresistive coefficient for (001) Si-plane [29]. $\Pi$ can be expressed as a function of fundamental Si piezoresistive coefficients ($\Pi_{11}, \Pi_{12}, \Pi_{44}$) and angles $\theta$ and $\phi$ as [26]:

$$
\Pi(\theta, \phi) = \Pi_{11} \cdot (\cos^2 \theta \cdot \cos^2 \phi + \sin^2 \theta \cdot \sin^2 \phi) 
+ \Pi_{12} \cdot (\cos^2 \theta \cdot \sin^2 \phi + \sin^2 \theta \cdot \cos^2 \phi) 
+ 2 \cdot \Pi_{44} \cdot \sin \theta \cdot \cos \theta \cdot \sin \phi \cdot \cos \phi
$$

(7)

For resistors oriented at $\theta = 45^\circ/135^\circ$ and uniaxial stress applied at $\phi = 0^\circ/180^\circ$, (7) becomes:

$$
\Pi(45^\circ, 0^\circ) = \frac{\Pi_{11} + \Pi_{12}}{2}
$$

(8)

The stress tensor $\sigma$ is expressed as a function of its in-plane components as:

$$
|\sigma| = \sqrt{|\sigma_{11}|^2 + |\sigma_{22}|^2}
$$

(9)

The above expressions have been used to setup the COMSOL simulator and to describe in Verilog-A the eight-resistor VHS model (discussed shortly) simulated in Cadence. Simulation results are presented in the following Section IV.

III. SYSTEM ARCHITECTURE

As mentioned in Section II-A, four versions of VHSs have been implemented on a single test chip. They are selectable through a multiplexer and dedicated switches, as shown in Fig. 1(e). Terminals $C_1$-$C_4$ are connected to each sensor depending on the value of the two digital inputs, $S_0$ and $S_1$.

A. VHSs Implementation

The four variants of VHS presented here were designed and fabricated in a 0.18-$\mu$m CMOS technology. The design parameters (Fig. 1(b)) include $L_C$, $L_S$, $D_C$, $D_S$, $W$ and $d$, which stand for centre contact length, side contact length, distance between centre and side contact, distance side contact from border of sensor, width and distance between the folds, respectively. The centre contacts are used for biasing and measurements while the side contacts connect the four folds of the device. The values of $L_C$, $L_S$, $D_C$, $D_S$, $W$ and $d$ used for the four realisations (namely, basic, small-distance, small-width, and deep n-well) are summarised in Table II. The basic sensor integrated on the chip acts as a reference. The small-distance and small-width sensors are scaled version of the basic device. The distance centre contact from side contact ($D_C$) and sensor width ($W$) have been modified, respectively. In the deep n-well sensor, the n-well active region has been replaced with a deep n-well.

B. Offset Reduction

A possible offset, which could occur due to mask misalignment during fabrication or mechanical stresses, can be reduced significantly by using the current spinning technique [30]. However, for voltage-mode driven Hall sensors, even after the current spinning operation, a small residual offset is still possible because of the junction field effect and the carrier velocity saturation, which may cause some non-linearity. This residual offset can be suppressed by the orthogonal coupling of four identical Hall sensors [17]. It may be noted that in the current mode, the voltage at the output terminals (common-mode voltage) remains constant. This means that the parasitic capacitances have little or no influence and, accordingly, the sensors show better linearity. This enables the current spinning technique to completely cancel any offset. A well laid out geometry of the Hall device can greatly decrease the offsets and improve the performance. For a 4F 3C VHS, the spinning circuitry design for two-phases operation has been reported in [31]. This design uses four phases, as shown in Fig. 1(f). The current spinning periodically interchanges the output and supply terminals of the VHS and allows rotation of the bias current injection and sink points in each state, while the offset appears at the output terminals. For instance, during $\Phi_1$ of Fig. 1(f), the bias current, $I_{bias}$, is injected into the terminal $C_1$ and the same bias current is drawn from another non-adjacent terminal, $C_3$. The two output currents, $I_{H_P}$ and $I_{H_n}$, are available at the other two terminals. Their difference gives the Hall current, $I_{Hall}$. During $\Phi_2$, the injection and sink terminals are $C_2$ and $C_4$, respectively, and $C_1$ and $C_3$ become the output terminals. At the end of the four phases, the offset is eliminated.

IV. SIMULATION AND MODELING

An eight-resistor Verilog-A compact model has been implemented to simulate the Hall sensor in Cadence environment together with the bias and the readout circuits. The model includes parameters to account for the sensor physical and mechanical properties estimated by means of FEM simulations. Accordingly, this Section presents the numerical results obtained by 3D simulations in COMSOL Multiphysics and compares them with those obtained in Cadence Spectre.

A. COMSOL Simulations

A 3D model of the current-mode VHS, based on the basic geometry described in Table II, has been implemented and simulated in COMSOL Multiphysics. Fig. 2(a) shows the configuration of the model geometry and the total displacement surface of VHS with substrate bending radii of 10 mm, when a magnetic field of 5 mT is applied. It can be noted that the maximum sensor displacement is less than 7.83 $\mu$m. This displacement changes the piezoresistivity of the sensor and appears as an offset at the output of the sensor.

To dynamically compensate for the offsets, mismatches due to substrate bending and possible masks misalignment during fabrication, the current-spinning technique has been used as described in Section III-B. The four configurations foreseen by the current-spinning technique (Fig. 1(f)) and the surface electrical distribution of the 4F 3C VHS with substrate bending are shown in Fig. 2(b). The applied magnetic field in this case is 5 mT. The simulation uses a nominal bias current of 10 $\mu$A. Fig. 2(c) shows the simulated current-mode sensitivity of the VHS when the magnetic field changes in the 0–5 mT range after the four current spinning phases and substrate bending.
radii in 10–25 mm range. The maximum differential output current (Hall current) is almost 4 nA for a magnetic field equal to 5 mT, as shown in the inset of Fig. 2(c). These current levels can be transformed into suitable voltages by integrating the current signal over a chosen period of time. A detailed description of the readout interface for magnetic sensors is given elsewhere [32]. Fig. 2(d) shows the simulated sensor output currents (Hall current) as a function of the magnetic field with 10 μA bias current after four current-spinning phases. In this case, the magnetic field varies from 0 to 5 mT with steps of 1 mT. The output offset of VHS due to substrate bending during these four phases can also be seen in Fig. 2(d).

B. Verilog-A Model

The COMSOL simulation of magnetic sensors by considering physics, geometry and technological constraints is the important first step for a system design. However, it is difficult to include in COMSOL simulations the secondary effects such as the presence of noise effects, parasitic capacitances, and electronics non-idealities. [33]. In this regard, Cadence environment is better as it allows optimization of the electronic front-end by considering non-idealities and sensor versus electronics interference. From a system viewpoint, these secondary effects should be considered in sensor modelling for better analyses of the overall performance. This is also needed to prepare a custom tool for the analog circuit design. The Verilog-AMS, a derivative of Verilog hardware descriptive language, which includes analog and mixed signal extensions to describe the behaviour of devices, is used here for further analysis. Specifically, the Verilog-A, which is a continuous time subset of Verilog-AMS, has been used here.

The VHS is simplified into a series of eight resistors, as shown in Fig. 2(e). Each contact terminal has two resistors, one on the left (RL) and another on the right (RR). At zero magnetic field, all resistors have the same initial value (R0). The Wheatstone bridge structure includes four electrical terminals (C1, C2, C3 and C4) and eight resistors (four RL and four RR). As per (6), the value of each resistor is a function of five parameters (R0, β, |B|, |σ|, Π). Furthermore, thanks to the device symmetry and to the fact that the sensor operates in current-mode, the effect of the junction field effect and of the carrier velocity saturation is considered negligible. Consequently, the PN junction effect is not included in this Verilog-A 8-resistors model.

The simulations were performed in Cadence using 10 μA input bias current and magnetic field in 0 to 5 mT range. To evaluate the accuracy of Verilog-A model, the simulation results have been compared with those obtained using COMSOL model for the basic VHS geometry. The Hall current can be obtained from differential current outputs at 5 mT as:

\[ I_{Hall} = I_{HP} - I_{HN} \]  

For a 5-mT magnetic field, the simulated \( I_{Hall} \) values in COMSOL and Cadence are 4.20084 nA and 4.20036 nA, respectively. These values are in excellent agreement. Using (1), the sensor sensitivity at a bias current of 10 μA is 8.4 [%T^{-1}]. This value is better than the range of sensitivity i.e. 1.5 – 4.3 [%T^{-1}] [14] reported in the literature for other VHSs [15], [16], [21].

V. MEASUREMENT RESULTS

The experimental results of the four different VHSs are discussed in this Section. First the design of the testing board and measurement setup are explained and then the measurement results are described. The prototype of the multi 4F 3C VHS was fabricated in a standard 0.18-μm CMOS technology. Fig. 3(a) shows the microphotograph of the chip with pads. The four sensors (basic, small-distance, small-width and deep n-well) and the multiplexer block are magnified. The whole chip occupies an area of 788 × 740 μm².
The prototype has 10 pins connected directly to the printed circuit board (PCB). Custom PCBs designed to test the prototype include a motherboard and a baby board. Fig. 3(b) shows the fabricated board with soldered components to test the prototypes in planar state. To prevent interference between the digital and analog parts, the motherboard uses two different power supplies, VDD and DVDD. These voltages are provided to the chip by means of two voltage regulators (LM4120) on the PCB. The PCB top and bottom plates are connected to VDD and to GND, respectively. The inject and drain bias current sources were provided by means of two current generators (LM234) on the motherboard. Two toggle switches are used as selectors. The main parts of the designed board e.g. current generators, voltage regulators and selectors have been highlighted in Fig. 3(b). The baby board uses a 80-pin socket (10 pins are connected to the chip) to hold the chip and for fast replacement of other samples during measurement. To generate a wide range of magnetic field, a Helmholtz coil with dimensions of 20 × 36 × 38 cm³ is also used.

The measurements were performed in voltage and current modes, as shown in Fig. 3(c)-(d). In voltage-mode the sensor was biased by a current generator. The Hall voltage \( V_{Hall} = V_{HP} - V_{HN} \) was obtained from the voltages \( V_{HP} \) and \( V_{HN} \), which appear at the two terminals shown in Fig. 3(c) when the external magnetic field is present. Fig. 3(d) shows the current-mode bias configuration of the sensor. For this measurement, two current generators (LM234) are used for obtaining the bias currents. Two off-chip low offset operational amplifiers (LF412) were used to fix the constant voltages \( V_{CM} \) at the output terminals.

For reliable operation of the sensor on flexible substrates, it is essential to examine the effect of bending on the failure limits of bonds with interconnects. In this regard, the limits of mechanical failure of VHS chip samples were investigated via experimental bending analysis. The experimental analysis was supported with the theoretical analysis using a finite element method, which was implemented in COMSOL and Verilog-A. For this purpose, the VHS chips were mounted and wire bonded on a 150-μm-thick double layer polyimide based flexible printed circuit (FPC) board. In fact, the sensors chip was also mounted on different flexible substrates i.e. a poly(vinyl chloride-co-vinyl acetate-co-maleic acid) (PVC), as shown in Fig. 1(a). Toward bending analysis of the chip on flexible substrate, the samples were fixed on clamps attached to a micrometer positioning system having moveable ends. The substrate undergoes bending when the movable ends are slowly moved towards each other, simultaneously, as shown in Fig. 3(e). Fig. 3(f) shows the current-mode and voltage-mode sensitivities versus substrate bending for different VHSs.

Table III summarizes the measured performance of the four different VHSs. From the measurement results, it is clear that the offset and sensitivity vary with geometry. The information for the current-mode and voltage-mode sensitivities are altered by changing the distance between contact terminals \( (D_C) \) and \( n \)-well width \( (W) \). To get a better voltage-mode sensitivity, the sensor width can be decreased. The small-width sensor device has the best voltage-mode sensitivity. In current-mode, the sensitivity can be improved by decreasing the contacts distances, and, with deeper \( n \)-well diffusion, this value will be ameliorated. The deep \( n \)-well and small-distance sensor devices prove to have the best performance in terms of current-mode sensitivity.

The residual offset, as per the current spinning technique described in Section III-B, can be calculated as:

\[
V_{OS,T} = \frac{V_{OS,\phi_1} + V_{OS,\phi_2} + V_{OS,\phi_3} + V_{OS,\phi_4}}{4}
\]  

(11)

where \( V_{OS,\phi_{1,2,3,4}} \) are the voltage offsets of the four current spinning phases. The magnetic field equivalent offset is defined as:

\[
B_{OS} = \frac{V_{OS,T}}{S_A} 
\]  

(12)

where \( S_A \) is the absolute sensor sensitivity, which is obtained by dividing the Hall voltage by the magnetic filed \( (S_A = I_{Hall}/B [A(T)^{-1}]) \). The offset measurements were performed in the absence of magnetic field after four phases of current spinning and have been evaluated at room temperature. The magnetic field for calculation of Hall voltage and absolute sensitivity is considered equal to 5 mT. Fig. 3(g) compares experimental results of the VHS devices in terms of current-mode and voltage-mode sensitivities and the magnetic
equivalent offset ($B_{OS}$). The average measured offset values are also annotated for each VHS. Among the four versions of VHS, the basic device presents the lowest magnetic field equivalent offset, $41.66 \pm 8 \mu T$. The highest offset is related to the deep n-well device with more than 500 $\mu T$. The substrate for the VHSs was bent to a maximum radius of curvature of 10 mm. The results indicate degradation of performance for the VHSs was bent to a maximum radius of curvature of 10 mm. The measurement results from more than 10 prototypes show that the basic device.

Table IV summarises the VHS performance for a bias current of 10 $\mu A$ and also provides a comparison of basic geometry device in this work with other recently published non-CMOS technology based flexible magnetic sensors.

VI. CONCLUSION

A magnetic sensors chip having four different VHSs and mounted on flexible substrates is presented in this work. The chip has been fabricated in a standard 0.18-$\mu$m CMOS process and mounted and wire bonded to two different polymeric substrates including PVC and polyimide-based FPC board. The optimal geometry of the Hall sensors on the chip has been investigated through simulations, which also consider the effect of mechanical stress on sensor performance. The results indicate degradation of performance by up to 2.5% when bending radius of curvature of the substrate changes from 10 to 25 mm. The measurement results from more than 10 prototypes show that the basic VHS achieves a sensitivity of more than 8% T$^{-1}$ over magnetic field range of 0-5 mT. The power consumption is in the range of $\mu W$. The use of the symmetric 4F 3C VHS and a current-mode approach allow offset cancellation with the current spinning technique.

Future work will involve thinning down the chip to $20 \mu m$ and integrating the sensor with a readout circuit in a single chip to increase the magnetic sensitivity. With integration of ultra-thin CMOS Hall sensors on a polymeric substrate, these sensors could find an attractive application in electronic skin and wearable electronics.

REFERENCES

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